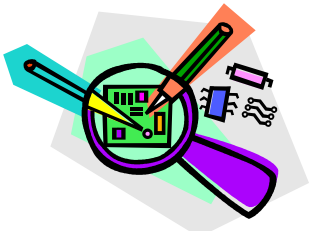
CSCI 3170 Computer Organization

Course Description

This course is a study of computer architecture and organization. Topics range from Boolean algebra and logic design, through microprocessor construction to performance enhancements.

Prerequisites: CSCI 1302

Textbook: Fundamentals of Digital Logic and Microcomputer Design
M. Rafiquzzaman
ISBN 0-471-72784-9



Grading: Scores on the following determine your final grade:

Test #1	25 %	
Test #2	30 %	
Final Exam	35 %	
Homework/Quiz	10 %	No late work accepted.

Course Grade Scale: After each exam, I adjust the grading scale if necessary.

A	92 -	100	
B	84 -	92	
C	74 -	84	
D	64 -	74	
F	0 -	63	

Attendance: You are strongly encouraged to attend class. I do not repeat lectures or provide notes. You are responsible for all class material whether or not you attend class. If you stop attending class, I have the right to withdraw you. However, withdrawing from the class is the responsibility of the student. Do not assume I will drop you from the class. If you stop attending after midterm, I will give you a WF.

Academic honesty is everyone's responsibility. Therefore, please familiarize yourself with the section on academic honesty in the GRU Student Manual and GRU Academic Policy. Academic dishonesty – cheating on exams, plagiarism of the work of others, unapproved collaboration on graded work, and the like – is not tolerated. Depending on the nature and severity of the problem, a student who is guilty of any such violation may be: 1) withdrawn from the course with a grade of WF (counted as an F in the GPA); 2) given a grade of zero on the assignment; 3) given a grade of F in the course; or 4) otherwise penalized, at the discretion of the faculty member.

Make-up Policy: No make-up exams are given. If, due to extraordinary circumstances, a student misses a class when an exam is scheduled, the instructor must be notified at least a week in advance unless it is some type of emergency. A student may be required to submit documentation. If the absence is an excusable absence, the weight of the missed exam is placed onto the final exam's weight.

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Office Hours: See Web page

Preliminary Course Outline*

Week	Book	Topics
1	1.5 1.6 2.1-2.2	Introduction History Number Systems and Codes Conversions
2	2.5.1 3.3	Binary Arithmetic Half Adder Gates
3	3.1-3.2,3.5 3.6 3.6	Boolean Algebra Rules and Theorems Circuit Design using Truth Tables Sum-of-Products Product-of-Sums Form
4	3.7 3.8 3.9	Karnaugh Maps Don't Cares, Gathering Zeros Quine-McCluskey Algorithm Circuits using NAND && NOR gates
5	 3.5.3 4 4.5.2 4.5.3	Time Response in Circuits Gate Delays Timing Hazards Combinational Logic Design Comparators Decoder
6	4.5.4 4.5.5 - 4.5.6 4.7 4.8 - 9	Encoder Multiplexer, Demultiplexer ROM PLD including PAL, PLA, FPGA
7	**Exam # 1**	
8	4.10, J.1	Hardware Description Languages
9	5 5.1 5.2.1	Sequential Logic Latches and Flip-Flops SR Latch
10	6.2.2 5.3 5.2.3 - 5	Clocks Master-Slave Flip-flop Edge-Trigger Flop-flops D, JK, T Flip-flop
11	5.11.1	Registers Shift Register Counters
12	5.6 5.9 5.7 5.10	Analysis of Sequential Logic Circuits Excitation and next-state equations Next-State Table and State Diagram Design of Sequential Logic Circuits Moore vs. Mealy Designing Counters
13	**Exam # 2**	
14	6.2.1	System Buses
15	 7.3.5	Data Path RTL
	Final Exam	

*Subject to change